A methodology to implement real-time applications on reconfigurable circuits

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Abstract

This paper presents an extension of our AAA rapid prototyping methodology for the optimized implementation of real-time applications onto reconfigurable circuits. This extension is based on an unified model of factorized data dependence graphs as well to specify the application algorihtm, as to deduce the possible implementations onto reconfigurable hardware, in terms of graphs transformations. This transformation flow has been implemented in SynDEx[1]*, a system level CAD software tool.*

1. Introduction

The increasing complexity of signal, image and control processing in embedded real-time applications requires high computational power to meet real-time constraints. This power can be achieved by high performance mixed hardware architectures, called "multicomponent", built from different types of programmable components (RISC or CISC processors, DSP,..) to perform high level tasks and/or specific non programmable components like (dedicated boards, ASIC, FPGA,...) used to perform efficiently low level tasks such as signal and image processing and devices control. Implementing these complex algorithms onto such distributed and heterogenous architectures while verifying the severe real-time constraints is generally a difficult and complex task. This explains the real need for dedicated high level graphical design environments based on efficient system-level design methodologies to help the real-time application designer to solve the specification, validation and synthesis problems [1].

[1] http://www-rocq.inria.fr/syndex

In order to cope with these increasing needs, in the one hand we have developped the AAA (Algorithm-Architecture Adequation) rapid prototyping methodology and the associated software tool SynDEx wich helps the real-time application designer to obtain rapidly an efficient implementation (i.e which meets real-time constraints and minimizes the architecture size) of his application algorithm on his heterogenous multiprocessors architecture and to generate automatically the corresponding distributed executive [2]. This methodology is based on graphs models in order to modelize the application algorithm, the available multiprocessors architecture as well as the implementation which is formalized in terms of transformations applied on the previous graphs.

In the other hand we aim to extend our AAA methodology to the hardware implementation of real-time applications onto specific integrated circuits, in order to finally provide a methodogy allowing to automate the implementation of complex application onto multicomponent architecture. This extension uses a single factorized graph model, from the algorithm specification down to the architecture implementation, through optimizations expressed in terms of defactorization transformations [3]. This optimization aims to satisfy the real-time constraints while minimizing the required hardware resources. In prospect, this extension is expected to allow the AAA methodology to be used for optimized hardware/software codesign and consequently to provide generation of either executives for the programmable parts of the architecture (network of processors), or structural synthesizable VHDL for the non-programmable parts (network of application specific circuits and/or FPGA).

This paper presents our extended methodology and is organized as follows. In Section 3, we briefly present the transformation flow used by our methodology to automate

the hardware implementation process of an application algorithm on reconfigurable circuits. First, we present in Section 4 the factorized data dependence graph model proposed to specify the application algorithm. In the next Section, a motivating example of matrix-vector product used to illustrate the methodology is described. We then present in Section 7 the principles allowing to automate the synthesis of both data and control paths from the algorithm specification. The principles of optimization by defactorization are shown in Section 8. We show also the results of the implementation of the matrix-vector product algorithm onto a *Xilinx* FPGA following these transformations. Finally, section 10 concludes and discusses future work.

2. Related Work

In the field of embedded real-time applications several system-level design methodologies have adressed the issues of design space exploration, performance analysis, mapping and optimizing applications onto different types of hardware architecture.

For example, the SPADE methodology [4] enables modeling and exploration of heterogeneous signal processing systems onto coarse-grain data-flow architectures. Applications can be structured starting from available C-code using the Khan API functions (the Khan Process Networks model is used to specify the application). SPADE design flow uses trace driven simulation to co-simule an application model with an architecture model.

SPARK [5] is a high-level synthesis framwework that provides a number of code transformations techniques. SPARK takes behavioral ANSI-C code as input and generates synthesizable RTL VHDL. This VHDL can then be synthesized into an ASIC or mapped onto an FPGA (the synthesized control is a finite sate machine controller).

GRAPE-II [6] is a system-level development environment for specifying, compiling, debugging, simulating and emulating digital-signal processing applications on heterogenous target plaforms consisting of DSPs and FPGAs. In the specification phase, the application is described using a cycle-static data flow. The application is represented as a directed graph, where nodes represent computation tasks, and edges the communications of the results (tokens). The fonctionality of the nodes is specified in conventional high level language (C, VHDL). The target architecture is specified as a connectivity graph. After specification, resources requirement, mapping architecture, the last phase generates C or VHDL code for each of the processing devices.

The POLIS system[2] implements a HW/SW codesign usign the CFSM (the Codesign Finite State Machine formal model). The related work in [7] describes the use of a statechart based tool for seamless specification and cosimulation of the entire CFSM network. A complete codesign environment, based on POLIS system, which combines automatic partioning and reuse of a module database is presented in [8]. Working on database of reusable software (C, assembler) and hardware modules (VHDL), the partitioning process passes back the allocation information into POLIS, where a first verification can be performed by Ptolemy[3] based simulation. Finally, the partitioning choice is verified, by using an emulator environment (CPU core coupled with FPGA boards).

Each methodology has its own features (for example several models can be used for application and architecture specification) and some of them have been improved. For example by introducing the statechart models into POLIS [7] the resulting CFSMs are smaller than those obtained via Esterel with POLIS. However, none of them take into account multicomponent architecture and use a unified model as well to specificy the application algorithm, as to deduce the possible implementation onto multicomponent architecture, and then to generate automatically the distributed executive corresponding to an efficient implementation (software and/or hardware implementations). Based on this unified model, we can generate both the data and control paths corresponding to hardware implementation.

3. AAA methodology for integrated circuits

Given an algorithm graph G_{al} specifying the application, we transform it into an implementation graph G_{im} following a set of graphs transformations as described in Figure 1. This transformation flow is composed of the generation of the data-path graph G_{dp} and the control-path graph G_{cp}. Data-path transformations are quite simple, but control-path transformations are not trivial and require to build first a neighborhood graph G_{ng}. Finally the implementation graph ($G_{im} = G_{dp} \cup G_{cp}$) containing both data and control graphs is charaterized in order to estimate time and surface performance of the implementation. If the deduced implementation does not satisfy the user specified constraints, we apply a defactorization process in order to reduce the latency by increasing the hardware ressources. Since there is a large but finite number of possible defactorized implementations, among which we need to select the most efficient one, we need to use heuristics guided by their cost function. Finally, the resulting optimized implementation is then used to generate automatically the corresponding VHDL code.

[2] http://www-cad.eecs.berkeley.edu/~polis/

[3] http://ptolemy.eecs.berkeley.edu/

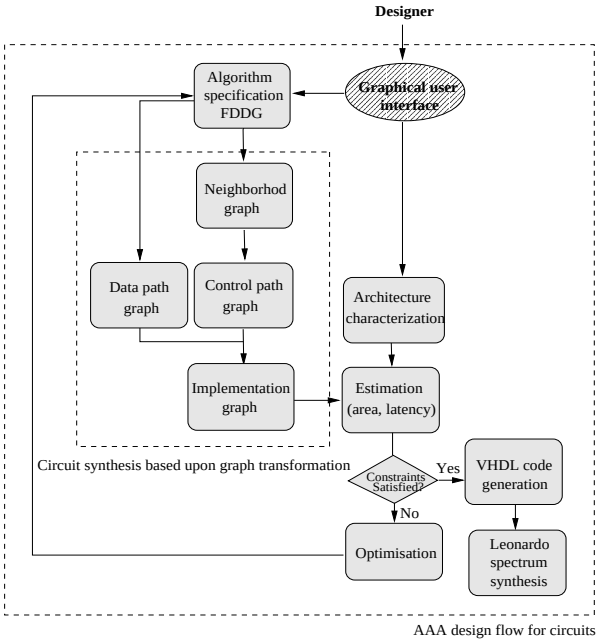


Figure 1. The AAA methodology for circuits

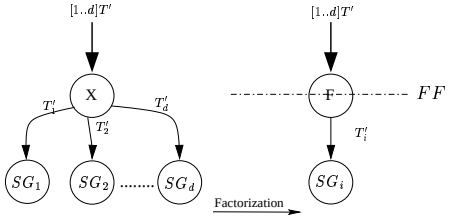
4. Algorithm model

The algorithm specification is the starting point of the process of hardware implementation of an algorithm application onto an architecture. According to the AAA methodology, the algorithm model is an extention of the directed data dependence graph, where each node models an operation (more or less complex, e.g. an addition or a filter), and each oriented hyperedge models a data, produced as output of a node, and used as input of an other node or several other nodes (data diffusion). Although the purely data dependence model is adequate for expressing the parallelism of computation which it is very attractive for real-time embedded applications, it is rarely sufficient for expressing iteration and repetition inherent in such applications. A more general data dependence model is thus needed. That is why, we extend the typical data dependence model to provide specification of loops through factorization nodes, leading to an algorithm model called Factorized Data Dependence Graph. In this FDDG model, each dependence is a data dependence and each node is either a computation operation, an input-output operation, or a repetitive operation. This algorithm graph may be specified directly by the user using the graphical or textual interface of the SynDEx software or it may be generated from high level specification languages. Such synchronous languages, Esterel, Lustre, Signal, perform formal verifications in terms of events ordering in order to reject specifications including deadlocks [9].

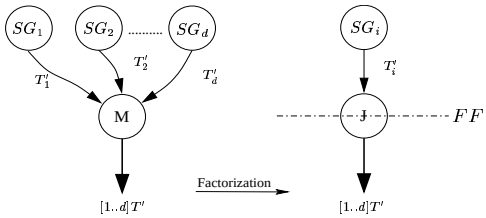
4.1. Factorized Data Dependence Graphs Model

In order to specify his algorithm the designer frequently has to describe repetitions of operation patterns (identical operations that operate on different data) defining a ”potential data parallelism”. To reduce the size of the specification and to highlight these regular parts we use in practice a graph factorization process which consists in replacing a repeated pattern, i.e. a subgraph (SG), by only one instance of the pattern, and in marking each edge crossing the pattern frontier with a special “factorization” node, and the factorization frontier (FF) itself by a dashed line crossing these nodes. The type of factorization nodes depends on the way the data are managed when crossing a factorization frontier. Then a factorization node may be:

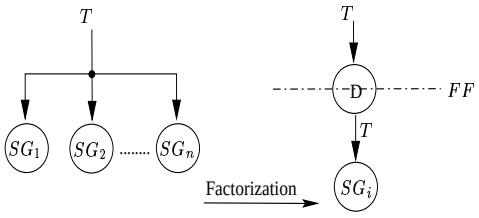
- **a Fork node (*F*)**: factorizes array partition by X in as many subarrays as repetitions of the pattern (subgraph SG);



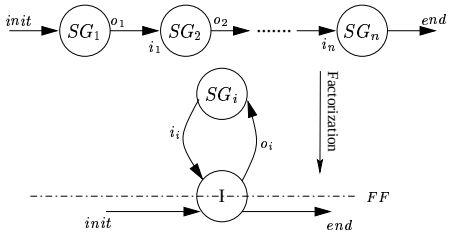
- **a Join node (*J*)**: factorizes array composition by M from results of each repetition of the pattern;



- **a Diffusion node (*D*)**: factorizes diffusion of a data to all repetitions of the pattern;



- **an Iterate node (*I*)**: factorizes inter-pattern data dependence between iterations of the pattern. The first of which takes its value from the init input, and the last of which gives value to the last output ’end’.



Note that the graphs in Figure 2 specify both the same scalar product SP of two integer vectors M_i and V of dimension 3, the one in figure 2.a is a non factorized data dependence graph and the one in Figure 2.b is the equivalent (from the specification point of view) factorized data dependence graph. In Figure 2.a the nodes X are an array-decomposition operation which separates its input array V (respec. M_i) into its elements. Althought apparently, Figure 2.a and Figure 2.b are not the same graph (different nodes and edges), they have the same semantics: apply the product operation mul as many times (3) as there are elements in the vectors to multiply and accumulate the sum. Thus, from the algorithm specification point of view, the factorization reduces only the size of the specification, without any modification of its semantic. However, from the implementation point of view, the factorization allows all the possible implementations, from the all parallel one to the all sequential one, with all the intermediate cases mixing both sequential and parallel. The factorized graph of Figure 2.b may be implemented of one of all its possible implementations. That is to say, an implementation where the three multiply operators will be executed sequentially through an iteration, or will be executed all in parallel like in Figure 2.a, or two of them will be executed in parallel and executed sequentially with the third one, etc. Obviously, each of these implementation will have different characteristics in terms of area and response time.

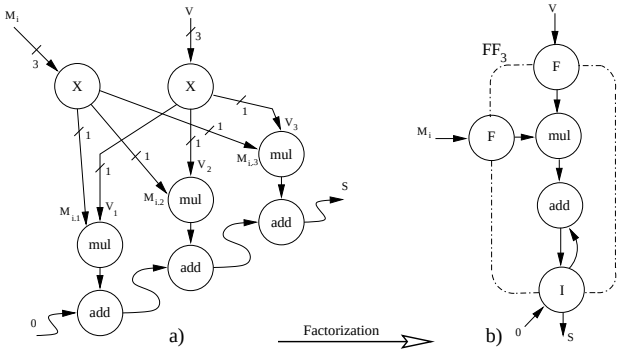


Figure 2. The factorization of a scalar product

5. Neighborhood graph

According to the data dependences relating the factorization frontiers, every factorization frontier may be a consumer (located downstream) or/and a producer (located upstream) relatively to another frontier. Two frontiers are neighbor if there is at least one relation of direct dependence that does not cross a third frontier.

Based on these neighborhood relations between the factorization frontiers in the algorithm graph G_{al}, we build a neighborhood graph G_{ng}. The nodes of such graph represent the factorization frontiers and the oriented edges represent the data flow between factorization frontiers. The edge orientation describes the consommation/production relation: an edge starts at a producer and ends at a consumer.

In the case of a sequential implementation of factorization nodes, every factorization frontier, called FF, separates two regions, the first one called "fast", being repeated relatively to the second one, called "slow". These slow and fast sides of a frontier are due to the difference of data transfer rate on each side of the factorization frontier. Every node of the neighborhood graph is then subdivided in four parts (see Figure 3):

- slow-downstream: "slow" side of a consumer FF;
- fast-upstream: "fast" side of a producer FF;
- fast-downstream: "fast" side of a consumer FF;
- slow-upstream: "slow" side of a producer FF.

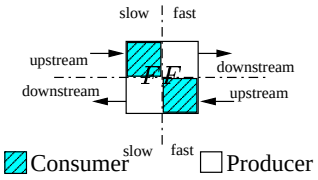


Figure 3. Node of neighborhood graph representing a factorization frontier FF

This neighborhood graph, deduced automatically from the FDDG, is then used during the implementation in order to establish the control relationships between frontiers.

6. Example: Specification of (MVP) Matrix-Vector Product

We now use a Matrix-Vector Product example (MVP) to illustrate the algorithm model of specification and its use for the building of the neighborhood graph. The choice of this example was motivated on the one hand because it presents

regular computation on different array data which highlight the use of the factorization process and on the other hand because it concentrates its computation in nested loops that manipulate multidimensional array data structures and such computations are of interest in signal and image processing applications. So the MVP of one matrix $M \in R^m \times R^n$ by a vector $V \in R^n$ gives a vector $C \in R^m$, and can be written in a factorized form as follows:

$$C = \left[\sum_{j=1}^{n} m_{ij} v_j \right]_{i=1}^{m} \quad (1)$$

where
m : number of lines of the matrix M,
n : number of columns of M, size of vector V,
m_{ij} : i-j-th element of the matrix M,
v_j : jth element of the vector V.

Equation 1 allows us to obtain the graph corresponding to the algorithm specification of the factorized MVP (Figure 4). The interface with the physical environment is delimited by input (F_M^∞ et F_V^∞) and by output (J_C^∞). It corresponds to the factorization frontier of the infinitely repeated pattern of the graph (FF_1) due to the reactive aspect of embedded real-time applications. Indeed, these applications interact infinitely with the physical environment by consuming data provided by sensors and producing data through actuators. The output data are the result of operations applied on the input data. The square brackets $[\ ]_{i=1}^{m}$ correspond to a second frontier (FF_2), delimited by factorization nodes of a finitely repeated pattern. This frontier selects the m lines of the matrix M (F_{21}), diffuses the vector V (D_{21}) and collects the result vector C (J_{21}). The functor $\sum_{j=1}^{n}$ corresponds to a third frontier (FF_3), also delimited by factorization nodes of a second finitely repeated pattern corresponding to the calculation of the scalar product $M_i V$. This frontier selects the m_{ij} elements of the ith line of the matrix M (F_{31}) and the elements v_j of the vector V (F_{32}) and it supplies the result of the sum of products between m_{ij} and v_j for every line of matrix M (I_{31}). The "slow" and "fast" sides of each frontier are labeled "s" and "f", respectively.

The neighborhood graph between factorization frontiers, obtained from the factorized data dependence graph specifying the MVP algorithm, is shown by the Figure 5. Because the factorization frontier FF_1 is infinite, it does not have neighbor on its "slow" side which corresponds to the physical environment. FF_1 is, at the same time, a producer (edges M and V) and a consumer (edge C) compared to FF_2. FF_2 is also a producer (edges M_i and V) and a consumer (edge C_i) compared to FF_3. FF_3 is a producer and a consumer, compared to itself through the arithmetic operations mul and add.

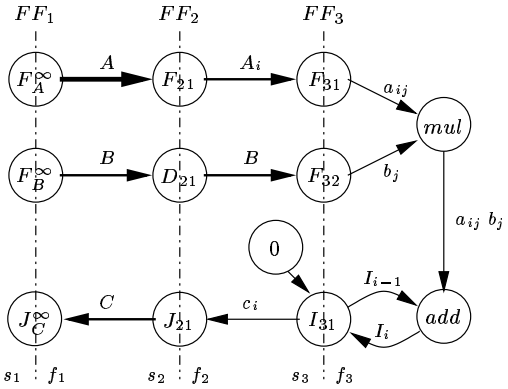


Figure 4. Factorized data dependence graph of MVP

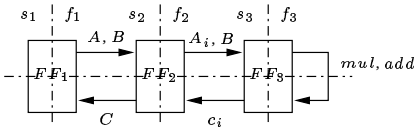


Figure 5. Neighborhood graph of MVP: relations between frontiers

7. Circuits synthesis

To implement the application algorithm on the corresponding circuit we need to generate the data path responsible for the core of the computation as well as control structure to generate the appropriate control signals. This translation process from a high-level behavioral representation into a register-transfer-level structural description (RTL) containing both the data and control paths is known as high-level circuit synthesis. The automation of this synthesis process reduces significantly the development cycle of the circuit, and allows the exploration of different hardware implementations, seeking for an ideal compromise between the area and the response time of the circuit. Afterwards, we will present principles allowing to generate automatically the data path and the control path of the circuit, from the factorized data dependence graph and the neighborhood graph.

7.1. Data path synthesis

The hardware implementation of the factorized data dependence graph consists in providing a matching operator for every operation node and every factorization node. The matching operator is a logic function in the case of an operation node, or it is composed of a multiplexer and/or regis-

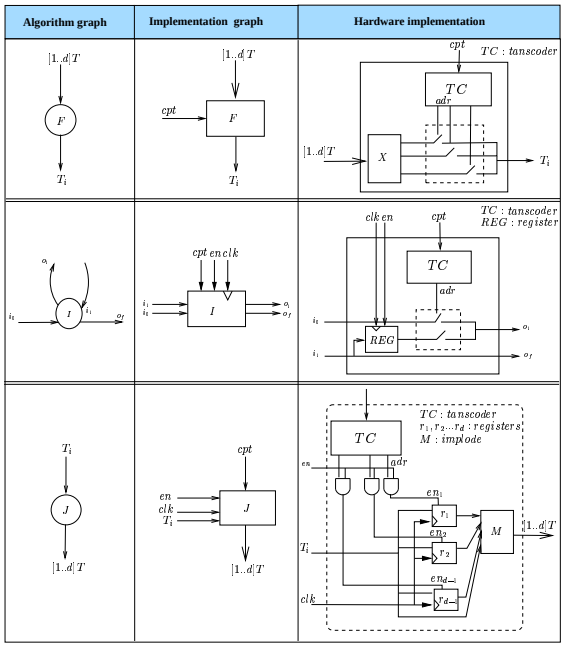


Figure 6. A node graph transformation: from algorithm graph to hardware implementation

ters in the case of a factorization node as depicted in Figure 6. Then hardware implementation of the data dependencies between operations consists in providing, for each edge of the graph, a matching connection between operators. The resulted graph of operators and their interconnections compose the data path of the circuit.

7.2. Control path synthesis

The control path corresponds to the logic functions that must be added to the data path, in order to control the multiplexers and the transitions of the registers composing the operators. It is then obtained by synchronization of data transfer between registers. However, two conditions must be satisfied to allow a register to change state: the new upstream data to the register must be stable, and all downstream consumers of the register must have finished the utilization of previous data. Moreover, if upstream data comes from various producers with different propagation time, it is necessary to use a synchronized data transfer process. This synchronization is possible through the use of a request/acknowledge communication protocol [10]. Consequently, the synchronization of the circuit implementing the whole algorithm is reduced to the synchronization of the request/acknowledge signals of the set of factorization operators. Given that these operators are gathered in factorization frontier and their data consumptions and productions are done in a synchronous way at the level of the frontier, the generated control must be a local control at each frontier. We propose then a local control system where each factorization frontier will have its own control unit. This delocalized control approach allows the CAD tools used for the synthesis to place the control units closer to the operators to control rather then a centralized control approach.

7.2.1 Control units and their interconnections

As mentioned above, each factorization frontier has upstream and downstream relations on both sides,"slow" and "fast". The relations between upstream/downstream and request/acknowledge signals on both sides of a frontier are implemented by the "control unit" of the factorization frontier (Figure 7). This control unit contains a counter C with d states (corresponding to the d factorized repetitions) and an additional logic function in order to generate, in the one hand the communication protocol between frontiers (the slow/fast, request/acknowledge signals at the upstream and downstream sides), and in the other hand the counter value (cpt) and the enable signal (en), that control the frontier operators. The counter value (cpt) controls the multiplexers of the frontier operators: F, J and I. The enable signal (en) determines the clock cycles where the registers of the frontier operators (F^{∞}, J^{∞}, J and I) will change state. Note that, the signal $(init)$ resets the counter while the signal (end) indicates that the counter is in its last state $(d-1)$.

All the other signals are the request (r) and acknowledge (a) signals generated by the frontier(s) located upstream or diffused to the frontier(s) located downstream. They are separated in two groups: those which relate to the frontier(s) located on the "slow" side and those which relate to the frontier(s) located on the "fast" side, corresponding to the four parts of the control unit: slow-upstream (su), slow-downstream (sd), fast-upstream (fu) and fast-downstream (fd).

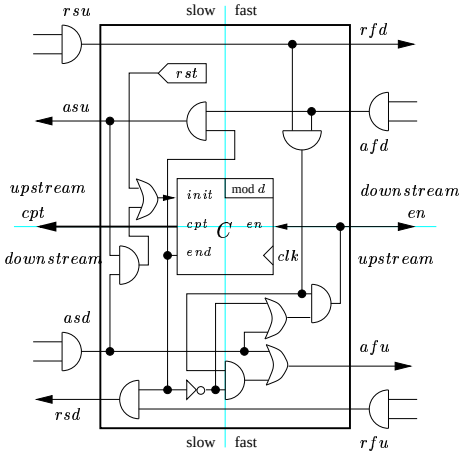


Figure 7. Control Unit

As mentioned above, the control path is mainly composed of the set of control units associated to the factorization frontiers of the application algorithm graph. These control units can then be inter-connected in an automatic way based on relationships between the factorization frontiers deduced from the neighborhood graph. In this control graph, the nodes correspond to the control units and the arcs correspond to the request signals transmitted between the control units in the same way as the production and consumption of data between the corresponding factorization frontiers. The acknowledge signals are transmitted, in the opposite direction of the associated request signals, between the same control units. When several signals arrive at the same input of a control unit, one takes the conjunction by a logical AND. In Section 9, we will see two examples of synthesis of the data and control paths.

8. Implementation optimization

If the implementation of the factorized specification onto an application specific integrated circuit or an FPGA does not meet the real time constraints, we need to defactorize the implementation graph corresponding to the specification. The defactorization process is the reverse transformation of the factorization and therefore it does not change the operational semantic of the data dependence graph. The goal is to obtain a more parallel implementation in order to reduce the latency and improve the temporal performances in spite of increasing hardware resources.

Thus the optimized implementation of a factorized algorithm graph onto the target architecture is formalized in terms of graph defactorization transformation. The implementation space which must be explored in order to find the best solution, is then composed of all the possible defactorizations of a factorized graph specifying the algorithm. For instance, for a given algorithm graph with n frontiers, we have at least 2^n defactorized implementations. Moreover, each frontier can be partially defactorized: a factorization frontier of r repetitions can be decomposed in r' factorization frontiers of r/r' repetitions.

Consequently, for a given algorithm graph, there is a large, but finite, number of possible implementations which are more or less defactorized, and among which we need to select the most efficient one, i.e. which satisfies the real-time constraints (upper bound on latency), and which uses as less as possible the hardware resources, logic gates for ASIC and number of Configurable Logic Blocks CLB for FPGA. This optimization problem is known to be NP-hard, and its size is usually huge for realistic applications. This is why we use heuristic guided by a cost function, in order to compare the performances of different defactorizations of the specification. This heuristic allow us to explore only a small subset of all the possible defactorizations into the implementation space.

Since we aim rapid prototyping, our heuristic is based on a fast but efficient greedy algorithm, with a cost function f based on the critical path length metric of the implementation graph: it takes into account both the latency T and the area A of the implemantation which are obtained by a preliminary step of characterization.

8.1. Optimization heuristic

Here is a brief description of the proposed greedy heuristic described by the algorithm 1. At each step, a list of candidate factorization frontiers FF_{list} is built from the set of factorization frontiers of the deduced implementation graph G_{im}. These frontiers are those which belong to the critical path CP. Defactorizing one of these frontiers will reduce the critical path length to meet the real time constraint C_t. Thus for each frontier $FF \in FF_{list}$ we determine its optimal defactorization factor df_{FF} as the smallest factor of factorization implying a latency lower than the time constraint C_t. When this factor corresponds to the factor of factorization (total defactorization) without latency being lower than the time constraint, then the fully defactorized factorization frontier is not crossed any more by the critical path.

Then we compute for each couple (factorization frontier FF, optimal corresponding factor df_{FF}) the cost function f, called defactorization pressure, as follow:

$$f = \frac{\Delta A}{T - max\{T', C_t\}}$$

where ΔA represent the loss on the area, T the latency before defactorization, T' the latency after defactorization and C_t is the user specified time contraint. At the end of each iteration, the factorization frontier having the highest cost value will be defactorized by its corresponding df_{FF}.

9. Example: Synthesis of MVP Implementation on FPGA's circuit

The Figure 8 represents the hardware implementation of the factorized MVP corresponding to the algorithm specification given in Figure 4 for $m = n = 6$. The data path (Figure 8.a) is composed of the factorization frontier operators ($F_{i,j}$, $D_{i,j}$, $J_{i,j}$ and $I_{i,j}$) and the combinatorial operators mul and add. The control path (Figure 8.b) is composed of the control units UC_1, UC_2 and UC_3, and of the control signals r(request), a(acknowldge), cpt and en. The interconnections between the request and acknowledge signals, is based on the relationships between the factorization frontiers, namely the neiborhood graph (Figure 5) built from the algorithm graph.

Algorithm 1 Greedy optimization algorithm

Inputs: The FDD graph G_{FDD}, time constraint C_t
Output: The optimized implementation graph

1: **begin**
2: If the latency of the corresponding implementation graph G_{im} meets the time contraint then go to end
3: Determine the list of candidates frontiers FF_{list} by computing the critical path CP;
4: For each candidate frontier $FF \in FF_{list}$ determine the optimal factor of defactorization df_{FF};
5: For each candidate frontier $FF \in FF_{list}$ compute its cost function f;
6: Defactorize the frontier having the highest cost by its corresponding defactor df_{FF};
7: Repeat 2 as long as the latency is greater than the time constraint;
8: **end**

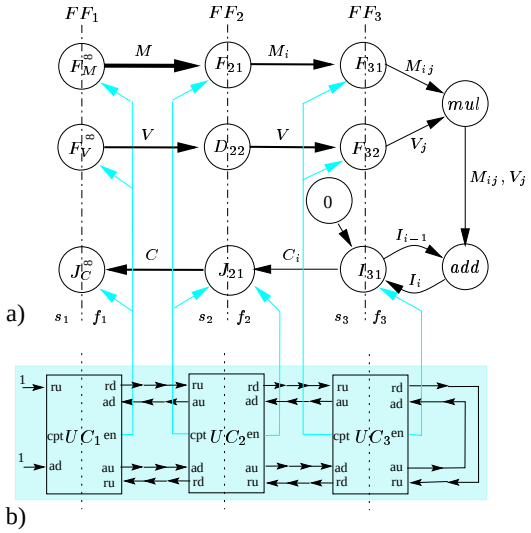


Figure 8. Implementation graph of MVP

In Figure 9.a we present the hardware implementation of a defactorized solution corresponding to the partial defactorization of the frontier FF_2 by a factor of 2. The $FF2$ frontier has been replaced by two frontiers FF_{2a}, FF_{2b}, each being repeated 3 times. The factorization frontier FF_3 remains unchanged but it has been duplicated (FF_{3a}, FF_{3b}) due to the partial defactorization of FF_2. The data path is then composed of the factorization frontier operators, the combinatorial operators (mul, add) and of the operators X (array-decomposition operation), M (array-composition operation). The control path, deduced automatically from the neiborhood graph (Figure 9.b), is composed of the control units UC_1, UC_{2a},UC_{2b},UC_{3a} and UC_{3b}. The synchronisation of frontiers FF_{2a}, FF_{2b} is assured by the AND gates at the upstream request and the downstream acknowledge of UC_1.

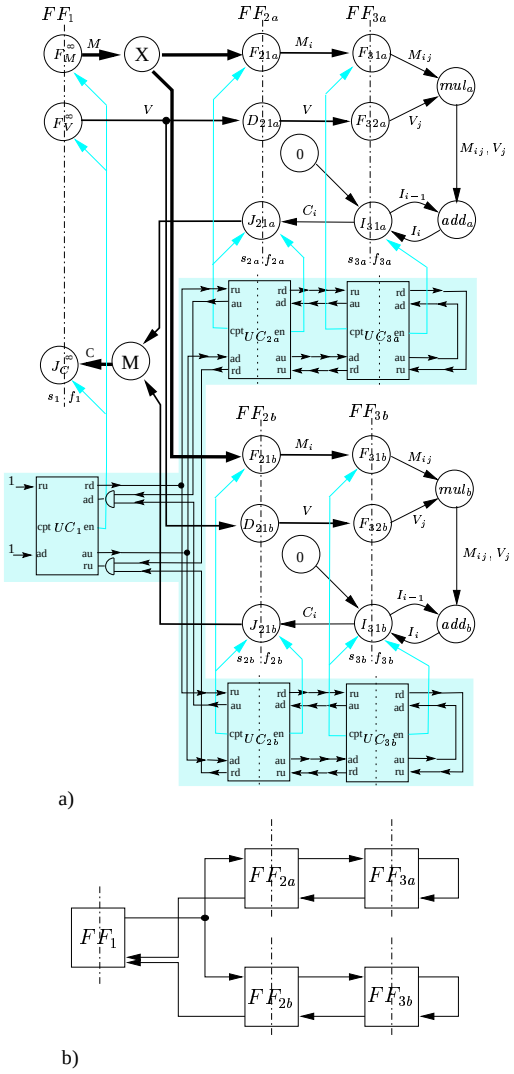


Figure 9. A defactorized implementation graph of MVP

Tab.1 shows the implementation results of hardware implementation of MVP (6×6 matrix and 6 elements vector, coded on 3 bits) onto a *Xilinx* FPGA XC4000XL-3, using the CAD tool *Leonardo Spectrum*, developed by *Exemplar Logic Inc.*. The implementation results are presented in function of, the area (hardware ressources: number of CLBs), the number of clock cycles required by the algorithm execution, the maximum frequency of operators in *MHz*, and finally the data latency in *ns* (nano seconds).

These results represent some possible implementations explored by the optimization heuristic by partial defactorization (as described in [3]) of the initial factorized implementation. Note that these defactorized solutions allow to

Table 1. Optimization results for the implementation of MVP onto FPGA

Implementation	*Area (CLB)*	*Nb. cycl.*	*Freq. (MHz)*	*Lat. (ns)*
Factorized Spec.	76	36	12,4	2916
Part.defac. by FF_2	99	18	13,5	1332
Fully. defac. by FF_2	168	6	14,3	420
Part. defac. by FF_3	92	30	10,8	2790
Fully. defac. by FF_3	79	6	9,0	660
Fully. defactorized	234	1	11,4	87

reduce the latency of the implementation, but they increase the number of required hardware ressources (CLB).

10. Conclusion and future works

We have presented a flow of transformations that lead to the generation of a complete VHDL design corresponding to the implementation of an application specified by Factorized Data Dependence Graph model. We validated the proposed methodology on several examples representative of low-level image processing such as mean filtering [3], edge detection operators: Deriche, Sobel,...

This work is part of the extension of the AAA methodology implemented in the software SynDEx to support implementation on reconfigurable circuits. Basically, AAA/SynDEx for multiprocessors, allows to generate automatically the dead-lock free executive for the optimized implementation of the given algorithm onto for architectures based on DSP (TMS320C40, ADSP21060), microcontrollers (MPC555), and general purpose processors (linux PC and unix workstations) [11].

The principles described in this paper allowed us to extend the AAA/SynDEx for reconfigurable circuits (FPGA). An automatic generator of structural synthesizable VHDL for mono-FPGA (one FPGA) architectures, has been added to SynDEx [12]. The generated VHDL code which corresponds to the optimized FPGA implementation obtained by successive defactorizations of the factorized algorithm graph, is then used by a CAD tool (e.g. *Leonardo Spectrum*) in order to generate the netlist needed for the FPGA configuration.

Presently we are working on the control involved by the conditioning in the algorithm specification, in addition to the control involved by repetition of operation. We intend to extend the proposed methodology to the case of multi-FPGAs architectures. To support such architectures, the optimization heuristic will adress both defactorization and partitioning issues.

Thanks to this extension, the AAA methodology will be used for optimized hardware/software codesign, leading to the generation of either executives for the programmable parts of the architecture (network of processors), or structural synthesizable VHDL for the non-programmable parts (network of application specific circuits and/or FPGA)

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