Adaptive Gain and Delay Mismatch Cancellation for LINC Transmitter

Corinne Berland, Jean-François Bercher, Olivier Venard

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Abstract LInear amplification with Nonlinear Component (LINC) transmitter architecture is an efficient solution for high efficiency amplification of signals. Nonetheless, this solution suffers both from gain impairment and delay mismatch between the two signal paths. Indeed, a mismatch in propagation time between the paths degrades the quality of the transmit signal but also disrupts the convergence of the gain correction algorithm resulting in a degradation of its performance. In this paper, we present an adaptive algorithm based on a gradient descent formulation for the identification and correction of these delays. We also demonstrate its effectiveness when applied prior to the gain adjustment procedure. The identification approach is preferred here, to ensure monitoring facilities.

Keywords Radio transmitters; power amplifiers; adaptive signal processing; delay filters; delay estimation; nonlinear distortion.

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1 Introduction

The high data rate demand for data transmissions in radio-communication systems implies the use of efficient modulation schemes for increasing the spectral efficiency of these systems. The use of non constant envelope modulations induces stringent constraints on the linearity and the efficiency of the transmitter. Thus, the choice of the transmit architecture is realized considering the feasibility of the analog front end and the additive digital signal processing necessary for achieving desired performances [1].

Among all the appropriate transmitter architectures, we find the LINC solution which is based on the separation of any modulated signal into two constant envelope phase modulated signals. These two signals follow two parallel paths and are recombined after efficient power amplification. However, this architecture is sensitive to mismatch between the two transmit paths: gain impairment and differences in propagation delays. The gain imbalance is a well known drawback of this topology and some solutions for solving this problem are presented in [2–5]. In addition to this gain mismatch, we demonstrate in this paper that the delay mismatch between the two paths has to be taken into account. It does not only degrade the output performances of the transmitter but also corrupts the gain correction by adding a time dependent perturbation on the phase.

In the first part of this paper, after a brief introduction to the LINC architecture and the impact of the delay mismatch on output performances, we will present a solution for delay adjustment based on the minimization of the quadratic error between the desired output signal and the emitted one. In the second part of this article, we will demonstrate the usefulness of this correction in addition to a gain mismatch correction between the two paths
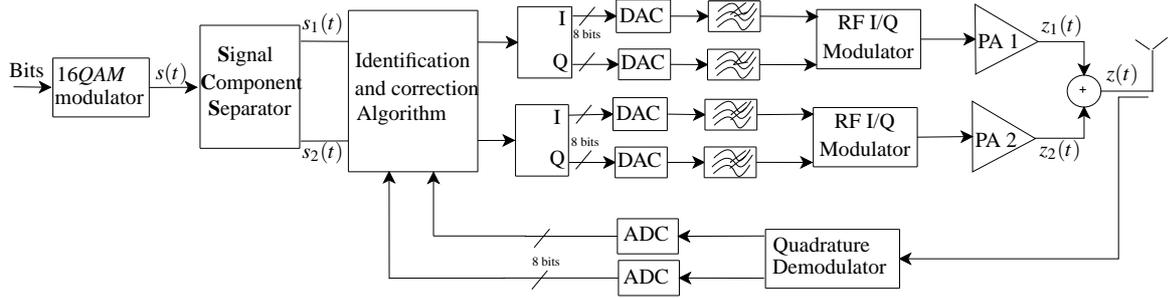
Fig. 1 Simulation model of the transmitter. This model includes an I/Q modulator signal component separator for the generation of the two constant envelope modulated signals. Both signals are converted into analog using 8-bit DAC and translated to RF with an I/Q modulator. The sum of the two signals is operated at the output of the PAs and a feedback loop (quadrature demodulation and 8-bit ADCs) is implemented for applying correction algorithms.

2 LINC transmitter

2.1 Principle of the architecture

The principle of the LINC transmitter [6] consists of rewriting any modulated signal as the sum of two constant envelope modulated signals, denoted by $s_1(t)$ and $s_2(t)$.

$$s(t) = s_1(t) + s_2(t).$$

After the frequency translation and efficient amplification stages, these two signals are added, with a combiner, so as to recover the original modulated signal.

The generation of the two constant envelope phase modulated signals is based on the following development: let us consider the band-limited modulated signal expressed using its complex representation,

$$s(t) = a(t) \exp^{j\phi(t)}, \tag{1}$$

with $\max[a(t)] = A_m$ and $a(t) = A_m \cos(\theta(t))$.

At the output of the SCS (Signal Component Separator), two phase modulated signals, $s_1(t)$ and $s_2(t)$, are generated with:

$$s_1(t) = \exp^{j(\phi(t) - \theta(t))}, \; s_2(t) = \exp^{j(\phi(t) + \theta(t))}. \tag{2}$$

These two signals can also be expressed as:

$$s_1(t) = \tfrac{1}{2}[s(t) - s_e(t)]$$

$$s_2(t) = \tfrac{1}{2}[s(t) + s_e(t)] \tag{3}$$

with

$$s_e(t) = js(t)\sqrt{\frac{A_m^2}{a^2(t)} - 1}. \tag{4}$$

This component separator can be implemented using either a digital processing unit or an analog approach as demonstrated in [7] and [8].

The model of the LINC transmitter developed in this article, Fig.1, is realized with Agilent ADS. This model takes into account quantization effects, with 8-bit DACs at a sample rate of $8F_s$. The output of these DACs are filtered with 5th order Butterworth filters before the quadrature modulation and the amplification. For the purpose of the study, RF delays are added in each path to model the desynchronization between the two signals. The feedback loop is implemented with a quadrature demodulator and two 8-bit ADCs at a similar sampling rate of $8F_s$.

2.2 Impact of delay mismatch

In this paper, we consider the performance of a transmitter according to the 3GPP standard using the 16QAM modulation for HSDPA with a chip rate of 3.84 *Mcps* [9]. Among all the scenarios specified in this standard, we will focus on the most stringent performance specifications. The output RF spectrum emissions are specified in term of Adjacent Channel Leakage power Ratio (ACLR). The specification of the ACLR is 33 *dB* at ±5 *MHz* from the assigned channel frequency and 43 *dB* at ±10 *MHz*. The EVM has to remain lower than 17.5 %. In the simulation model implemented, without any desynchronization, the EVM value is 0.3 % and ACLR at ±5 *MHz* and ±10 *MHz* are respectively 43 *dB* and 53 *dB*.

To evaluate the impact of delay mismatch between the two paths, we introduce a differential delay. The results of simulations are given in Table 1, where T_s is the duration of an emitted symbol at the output of the modulator (this is in fact the chip time of the standard) and is equal to $T_{chip} = T_s = 1/3.84e6 \approx 260 \, ns$. From these results, it is obvious that both EVM and ACLR are impacted: $T_s/32 \approx 8 \, ns$ seems to be the limit of acceptance for the delay, without any margin for other impairments in this architecture. Therefore delay compensation is mandatory.

Table 1 Impacts of differential delay mismatches on the EVM and on the spectrum.

Delay	EVM (%)	ACLR @ ± 5 *MHz*
$T_s/64$	1.6 %	38 dB
$T_s/32$	3.2 %	32 dB
$T_s/21$	5 %	28 dB
$T_s/16$	6.8 %	26 dB
$T_s/13$	8.8 %	24 dB
$T_s/10$	10.7 %	22 dB
$T_s/9$	12.1 %	21 dB
$T_s/8$	13.5 %	20 dB

3 Delay Adjustment

In this section we present a delay identification algorithm in order to cancel mismatch, and so, improve the performance of the transmitter.

3.1 Synchronisation algorithm principle

Let us consider that $s_1(t)$ is delayed by τ_1 whereas $s_2(t)$ is delayed by τ_2, with $\tau_2 - \tau_1 = \Delta$. At the output of the transmitter, considering these delays, the original modulated signal $s(t)$ is modified to give $z(t)$:

$$z(t) = z_1(t) + z_2(t)$$
$$= s_1(t - \tau_1) + s_2(t - \tau_2) \tag{5}$$

This can be rewritten as:

$$z(t) = \frac{1}{2} \left[\underbrace{s(t - \tau_1) + s(t - \tau_2)}_{1} \right. $$
$$\left. + \frac{1}{2} \left[\underbrace{s_e(t - \tau_2) - s_e(t - \tau_1)}_{2} \right] \right]. \tag{6}$$

The first term of this expression corresponds to the linear interpolation of $s(t)$ at the time $t - \tau_1 + \frac{\Delta}{2}$, the second term is the first order derivative of $s_e(t)$ at the time $t - \tau_1 + \frac{\Delta}{2}$. In order to compensate for these delays, a feedback loop associated with an adaptive algorithm is one solution. The aim of the algorithm is to reduce the quadratic distance between the original signal, $s(t)$, and the emitted one, $z(t)$.

Two solutions for the implementation can be explored. The first is to advance directly the emitted signal by values $\mu_1 = \tau_1$ and $\mu_2 = \tau_2$ so that the various delays are canceled: this is a correction algorithm. This approach is similar to the one presented in [10] for gain correction. One of the drawbacks of this solution is the need for an additive SCS in the feedback loop. Moreover, this solution is restricted to real time correction that precludes any monitoring capabilities.

The second solution resolves the values of τ_1 and τ_2: this is the identification procedure. Once the identification is done, the correction could be applied, if necessary. This implementation allows both correction and monitoring. Finally, the identification procedure presents the advantage of avoiding the use of an additive SCS. Advancing or delaying the signal is of course only possible if the transmitter introduces a delay between the emitted signal and the output of the modulator with a buffer. Moreover, the solution for delaying or advancing signals by fractional amounts relies on the use of interpolation filters which allow to adjust the delay without modifying the implementation of the filter [11], [12]. The choice of this interpolator has to be studied further because it impacts directly the value of the interpolated signal EVM. For this reason, we choose to implement a fifth order Lagrange interpolator using the farrow structure [13].

3.2 Derivation of the delay identification algorithm

Let us now study the formulation of the algorithm. If we denote $e(t) = z(t) - s(t)$ the error function we want to minimize, the gradient algorithm consists of iterating the searched value as follows:

$$\mu(k+1) = \mu(k) - \gamma(k) \left. \frac{\partial J(\mu)}{\partial \mu} \right|_{\mu = \mu(k)}$$

with $J(\mu) = \mathrm{E}\left[|e(t)|^2\right]$ being the mean square error and γ the adaptation step. Rewriting the expression of the derivative of the mean square error brings to:

$$\frac{\partial J(\mu)}{\partial \bullet} = \frac{\partial \mathrm{E}\left[|e(t)|^2\right]}{\partial \bullet} = 2\mathrm{E}\left[\Re\left(\frac{\partial e^*(t)}{\partial \bullet} e(t)\right)\right]$$

For the identification of the delays introduced by the transmitter, the algorithm will resolve μ_1 and μ_2 values such as:

$$s_1(t - \mu_1) = z_1(t)$$
$$s_2(t - \mu_2) = z_2(t) \tag{7}$$

This procedure is illustrated Fig.2. Considering the error to be of the form:

$$e(t) = z(t) - s_1(t - \mu_1) - s_2(t - \mu_2),$$

the derivative of the mean square error can be written as:

$$\frac{\partial J(\mu_1, \mu_2)}{\partial \mu_i} = \frac{\partial \mathrm{E}\left[|e(t)|^2\right]}{\partial \mu_i}$$
$$= -2\mathrm{E}\left[\Re\left[e(t) \frac{\partial s_i^*(t - \mu_i)}{\partial \mu_i}\right]\right] \tag{8}$$

The final formulation of the gradient algorithm is, with $i = 1, 2$,

$$\mu_i(k+1) = \mu_i(k) + 2\gamma(k)\Re\left[e(t) \left. \frac{\partial s_i^*(t - \mu_i)}{\partial \mu_i} \right|_{\mu_i = \mu_i(k)}\right].$$

This procedure then consists of finding the values of these two delays μ_1 and μ_2. Once these delays are identified, the
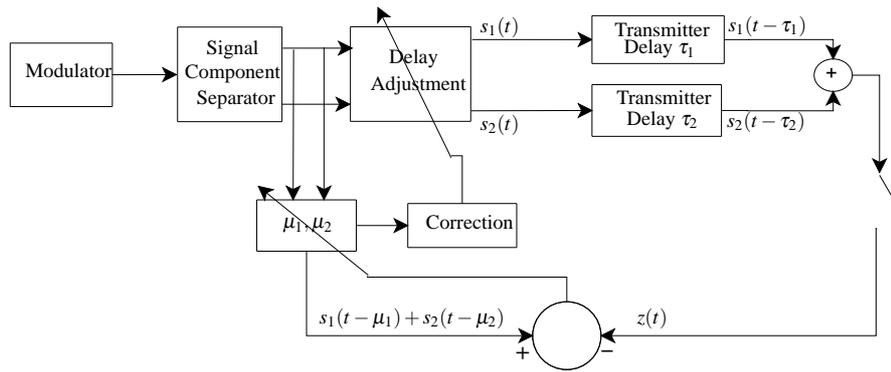
Fig. 2 Identification architecture : delay μ_1 and μ_2 are adjusted to cancel the quadratic error. After convergence, the correction is calculated and applied.

correction would have to be applied to the transmit path. It is worth noting that the algorithm not only identifies differential delay mismatch but also the global delay introduced by the analog front end. If the global delay introduced in the transmitter is acceptable for the application, the correction may be only differential and operated on a single path instead of being absolute for the two paths.

3.3 Simulation results

The convergence time for the identification procedure is illustrated Fig.3, for the same test cases as the ones given in Table 1, with a pseudo-random sequence at the input of the modulator. In the simulation scenarios, the differential delay, Δ, was only applied on τ_1. Both delays μ_1 and μ_2 are iden-
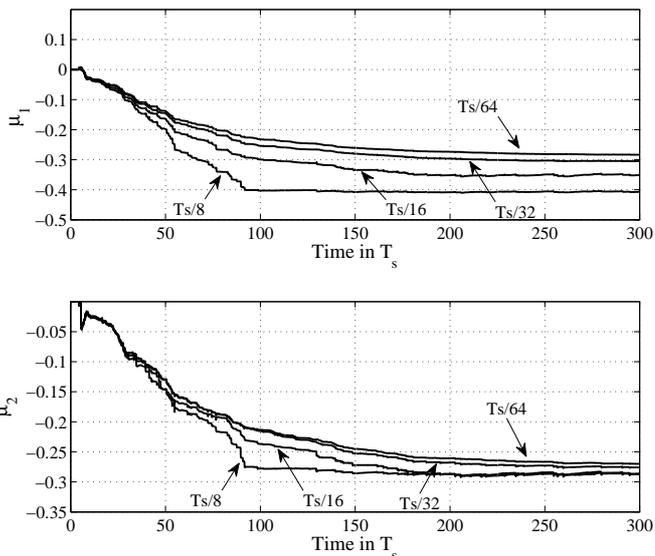

Fig. 3 Identification of μ_1 and μ_2 normalized to the symbol time, for $\Delta = [T_s/64, T_s/32, T_s/16, T_s/8]$

tified and the results take into account both, global propagation time linked to the baseband filters and the differential

delay mismatch. After $300T_c \approx 100~\mu s$ the convergence is obtained. The correction is then applied (by delaying or advancing one path relative to the other) and this allows, for all cases, the reduction of the EVM to 0.6 % with an ACLR at $\pm 5~MHz$ higher than 43 dB. The output spectrum after correction is shown in Fig.4. The dramatic improvement of the performance compared to the values given in Table 1 highlights the effectiveness of this delay equalization algorithm.
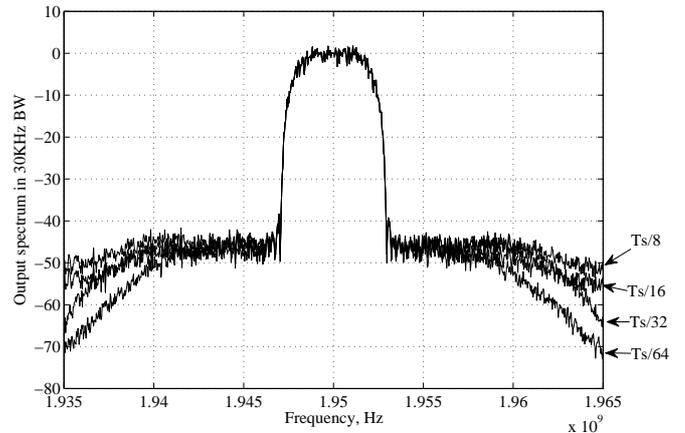

Fig. 4 Output spectrum after identification and correction of the delays, for $\Delta = [T_s/64, T_s/32, T_s/16, T_s/8]$

4 Gain and delay adjustment

In this section, we will now present the gain identification algorithm and demonstrate the necessity to realize a delay identification before applying a gain correction procedure.

4.1 Gain adjustment algorithm

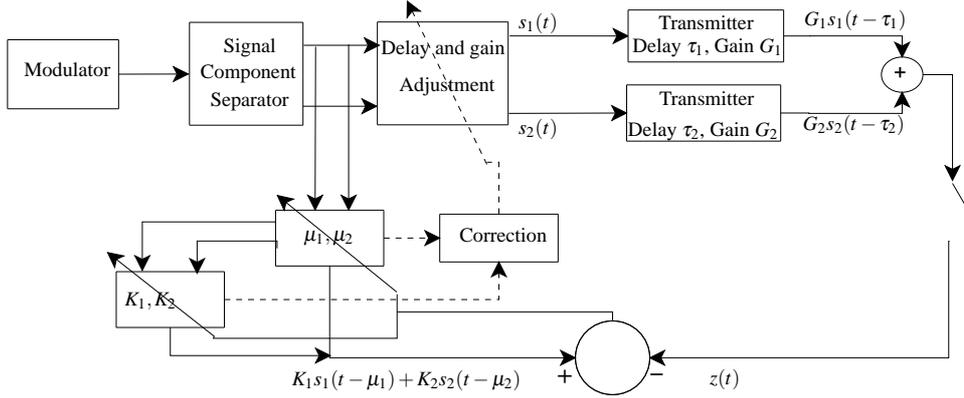Due to the non-linear operation on the modulated signal for the generation of the two constant envelope signals, we

Fig. 5 Gain and Delay mismatch cancellation architecture : delay μ_1 and μ_2 are identified ($K_1 = K_2 = 1$), corrected. The gain mismatch identification is realized in a second step. After convergence, the gain correction is applied.

choose to apply for the gain correction the same identification procedure as presented previously for the delay adjustment. Indeed, direct correction solutions as in [10] are only valid if we consider that the SCS in the return path gives at its output $z_i(t) \propto s_i(t)$: inspection of the formula suggests that this assumption is not valid for all types of signals. The output signal $z(t)$, see Fig.5, has now the following form, with G_1 and G_2 the two complex gains:

$$z(t) = G_1 s_1(t) + G_2 s_2(t).$$

The objective of the algorithm is to find K_1 and K_2 so that we minimize the quadratic error:

$$J(K_1, K_2) = E\left[|K_1 s_1(t) + K_2 s_2(t) - z(t)|^2\right].$$

This gives, for $i = 1, 2$:

$$\Re(K_i(k+1)) = \Re(K_i(k)) + 2\gamma_k(k)\Re[e(t)s_i^*(t)],$$

and

$$\Im(K_i(k+1)) = \Im(K_i(k)) + 2\gamma_k(k)\Re[j.e(t)s_i^*(t)].$$

As already highlighted in the introduction, the gain correction cannot be correctly achieved without a preliminary synchronization between the reference and the emitted signal. We introduced a gain and phase mismatch of 0.5 dB and 5° in the transmitter Fig.1 with no additional differential delays in both transmit paths than the one introduced by the analog filters. The ACLR is about 30 dB at 5 MHz and the EVM is approximately 5.9 %. Without any preliminary identification of the processing delay in the transmit path, the gain correction algorithm fails to converge. This is due to the fact that the algorithm tries to cancel, with the two complex gain phase values, a delay comprising the analog front end time processing and the phase value of both complex gains. If we simply identify this processing delay (ideal case here) and add it in the simulation before gain identification, the ACLR is higher than 43 dB and the EVM lower than 0.6 % after

the identification and correction of those two complex gains. This demonstrates the usefulness of the delay synchronization before the gain identification procedure even if there is no differential delay mismatch between the two paths.

The algorithm is implemented as follows, see Fig.5:

 – Identification of the delays
 – Correction of the delays
 – Identification of the complex gains
 – Correction of the complex gains

In our simulation environment, we choose to apply the delay correction after a convergence time of $500 Ts$.

4.2 Results of simulation

Further simulations were realized including both delay mismatch and gain impairment. We introduced a differential delay mismatch of $Ts/32 \approx 9$ ns between the two paths: this corresponds to a mismatch of 10 % of the propagation time between the two analog filters. A comparison of results was realized between the performance before the correction, after only a simple non differential delay identification (theoretical value taken for processing time in our simulated analog front end) and finally with the differential delay adjustment procedure. Results given in Table 2 demonstrate the efficiency of a differential delay correction as this allows a reduction of about 15 dB on ACLR and lowers the EVM to less than 1 %. It should be pointed out that for greater mismatch (above 1 dB and 15°) the algorithm exhibits poorer results in term of ACLR and EVM.

5 Conclusions

This paper addresses the sensitivity of the LINC transmitter architecture to impairments between the two transmit paths. In Addition to gain mismatch, we consider the impact of mismatch in analog processing delays and we evaluate its effects on the transmitter performances.

Table 2 Algorithms performances with and without differential delay adjustment, with $\Delta = \tau_1 - \tau_2 = T_s/32$

		Before		Without Diff Delay Adj		With Delay Adj	
ΔG	$\Delta \phi$	EVM (%)	ACLR	EVM (%)	ACLR	EVM (%)	ACLR
$0.1dB$	2°	4.2 %	27 dB	3.7 %	28 dB	0.7 %	43 dB
$0.2dB$	5°	6.9 %	23 dB	3.7 %	28 dB	0.8 %	41 dB
$0.5dB$	5°	6.9 %	23 dB	3.8 %	28 dB	0.7 %	41 dB
$0.6dB$	8°	10.8 %	20 dB	3.8 %	28 dB	0.8 %	40 dB
$0.8dB$	10°	14.1 %	18 dB	3.8 %	28 dB	0.9 %	39 dB

A solution to identify delays in each transmit path is proposed. This allows the identification of the global processing delay in the transmitter and also the correction of the differential delay impairments between the two paths. As the loop delay impacts the convergence of the gain correction solution, a two step solution is adopted: first an identification of paths processing time with a correction of the differential delay and then an identification and a correction of the gain mismatches. The proposed approach allows drastic improvement for both EVM and ACLR: in our test case it reduces the EVM from 14 % to 1 % and improves the ACLR at ± 5 MHz by more than 20 dB (from 18 dB to 39 dB for instance in the worst test case).

Acknowledgment

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